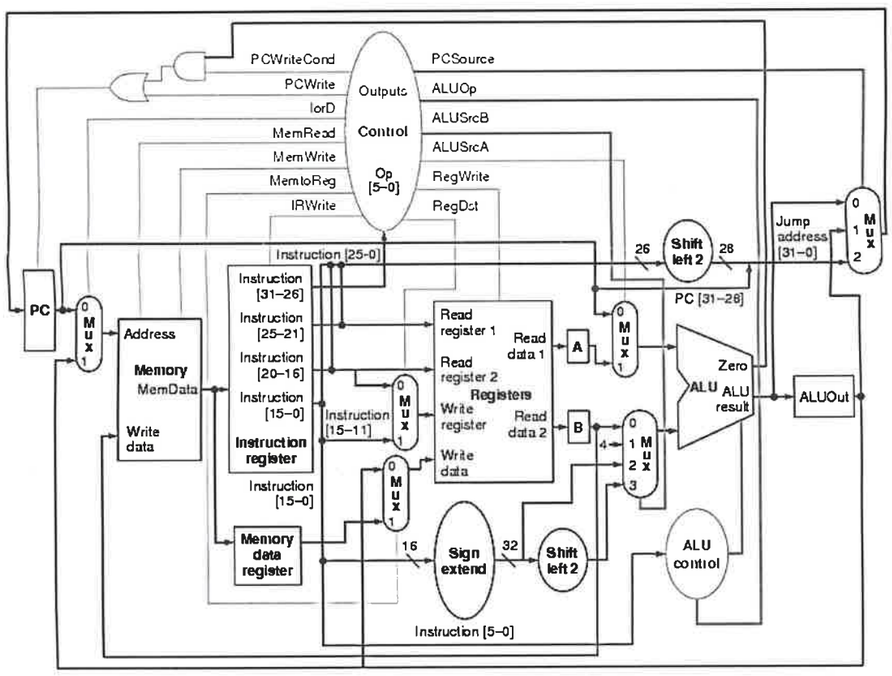
考試時間	月 日上午 下午第 節 (星期) 晚間	份數		任課教師	

國立臺灣科技大學 108學年度第 2 學期 考試命題用紙 第 1 頁共 3 頁

考試科目：Computer Architecture ☑研究所 ☐大學部 ☐工程在職進修 系班別：博士班資格考

1. Given a hierarchical memory system, assume the cache total data size is 8 MB and the memory size is 2^{30} bytes.
(A) If the cache system is implemented in direct-mapped cache with 8 words per block, how many tag bits are required? (3%)
(B) If the cache system is implemented in 4-way set associative cache with 8 words per block, how many tag bits are required? (3%)
(C) Assume that the cache hit access time is 1 cycle and the cache hit ratio is 95%. If the memory access takes 50 cycles and the memory to cache transmission takes 1 cycle, how many data access cycles are required from CPU to cache in average? (3%)
PS: 1 word = 4 bytes

2. There are several control signals in a multi-cycle processor implementation. These signals are PCWriteCond, PCWrite, IorD, MemRead, MemWrite, MemtoReg, IRWrite, PCSource, ALUOp (2-bits), ALUSrcB, ALUSrcA, RegWrite, and RegDst. Please fill up some of the aforementioned control signals of the add immediate instruction (addi) in every cycle. Use 'X' to represent the don't care condition of the control signal. (26%)



ALUop (Symbolic)	R-type	Add	Subtract	xxx
ALUop <1:0>	10	00	01	xxx

Cycle	PCWrite	IorD	MemRead	MemtoReg	IRWrite	PCSource	ALUOp	ALUSrcA	ALUSrcB	RegWrite	RegDst
1											
2											
3											
4											

命題請勿超出線外

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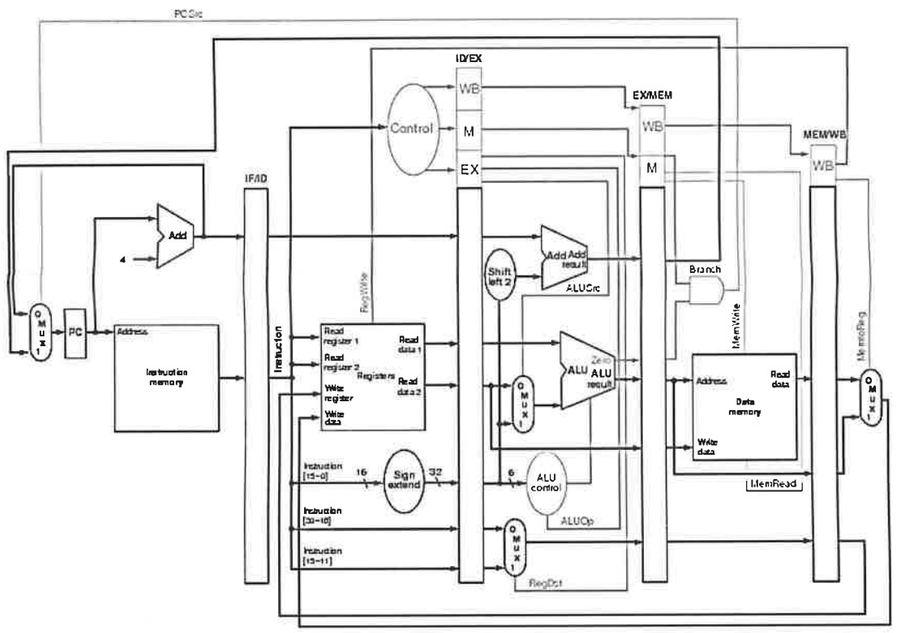
考試科目：Computer Architecture ☑研究所 ☐大學部 ☐工程在職進修 系班別：博七班資格考

3. In a MIPS pipeline processor design, we divide one instruction into five stages, instruction fetch (IF), instruction decode and register fetch (ID/RF), execution (EX), memory access (MEM), and write back (WB). Given a segment of MIPS instructions below, please answer the following problems.
(A) What is the instruction memory doing during cycle 3? (3%)
(B) What is the register file doing during cycle 6? (3%)
(C) What is the ALU doing during cycle 7? (3%)
(D) At which cycle the data memory is accessed? (3%)
(E) How many cycles are required to complete these instructions? (3%)

```
lw  $10, 20($1)
sub $11, $2, $3
and $12, $4, $5
or  $13, $6, $7
add $14, $8, $9
```



命題請勿超出線外

4. Suppose you have a machine which executes a program consisting of 50% floating point multiply, 20% floating point divide, and the remaining 30% are from other instructions.
(A) Manager wants you to improve the machine to run 4 times faster. Suppose you can make the following decisions, one is "the divide runs at most 3 times faster", the other is "the multiply runs at most 8 times faster". Could you meet manager's goal by making only one improvement? If yes, which one? If no, why? (5%)
(B) Now if you can make both the multiply and divide improvements, what is the speedup of the improved machine relative to the original machine? (5%)

5. Assume the following assembly code is run on a machine with 2 GHz clock rate, and the number of cycles for each assembly instruction is shown in the following table. Suppose that $a0=3, $a1=20 at the initial time.

```
        add  $t0, $zero, $zero
loop:   beq  $a1, $zero finish
        add  $t0, $t0, $a0
        addi $a1, $a1, -1
        j    loop
finish: addi $t0, $t0, 100
        add  $v0, $t0, $zero
```

Instruction	Cycles
add, addi, sub	1
lw, beq, j	2

(A) What is the value of $v0 after the execution of the final cycle? (4%)
(B) How many instructions will be executed for this assembly code? In other words, please calculate the total number of instruction count for executing this code with the given initial settings of registers. (4%)
(C) How many clock cycles will be required for executing this assembly code? (4%)
(D) What is the average CPI? (4%)
(E) What is the MIPS (millions of instructions per second) of this assembly code? (4%)

6. Please answer the following questions about IEEE 754 binary representation. Assume that only the single precision format is considered.
(A) What is the IEEE 754 binary representation of zero in the single-precision format? (4%)
(B) What are the maximum and the minimum positive numbers, excluding infinity, NaN, and denormalized numbers, in IEEE 754 binary representation? (4%)
(C) What are the maximum and the minimum negative numbers, excluding infinity, NaN, and denormalized numbers, in IEEE 754 binary representation? (4%)
(D) What are the maximum and the minimum positive numbers, excluding infinity and NaN, in IEEE 754 binary representation? (4%)
(E) What are the maximum and the minimum negative numbers, excluding infinity and NaN, in IEEE 754 binary representation? (4%)